



Doug Grose
Senior Vice President,
Manufacturing and Supply Chain
Management

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A Model That Supports AMD Objectives

Customer-Centric Innovation

AMD continues to reorient its business and the priorities of our industry around the needs of the customer

Operational Accuracy and Agility

To sustain and grow customer satisfaction, AMD continues to build an operational model that enables the right solutions, to be delivered at the right time, at the right price. Asset Smart is in place and continues to expand as our strategy develops

Honing every aspect of AMD operations to increase customer value by maximizing...

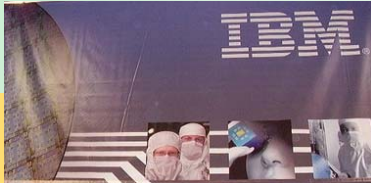

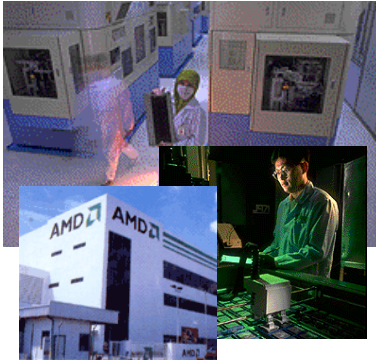


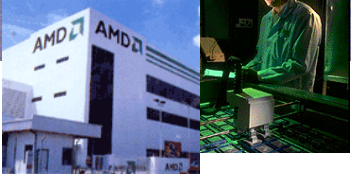
LEAN

Design for
Manufacturability
(DFM)

Factory
Automation
and flexibility

Return on
R&D

Manufacturing and R&D Model

	Base Material	Development / Research	Fab	Assembly / Test
MPUs	SOI <ul style="list-style-type: none"> • High Performance • Low Power • Scaleable • High Density 	IBM 	Fab 36 / 38 & Chartered 	AMD Penang Suzhou Singapore 
Visual & Media	Bulk Silicon <ul style="list-style-type: none"> • Low Cost • Broad Supply Base • Ideal for all but Highest Performance 	TSMC & UMC 	TSMC, UMC & Chartered 	External 

Process Technology R&D

AMD/IBM Development Alliance

Shared objective

- Production-ready high performance microprocessor technologies

Shared investment

- Early-stage research and development through 22nm generation
- AMD on-site team has grown from 15 to 70 since 2002
- “Asset Smart” technology R&D

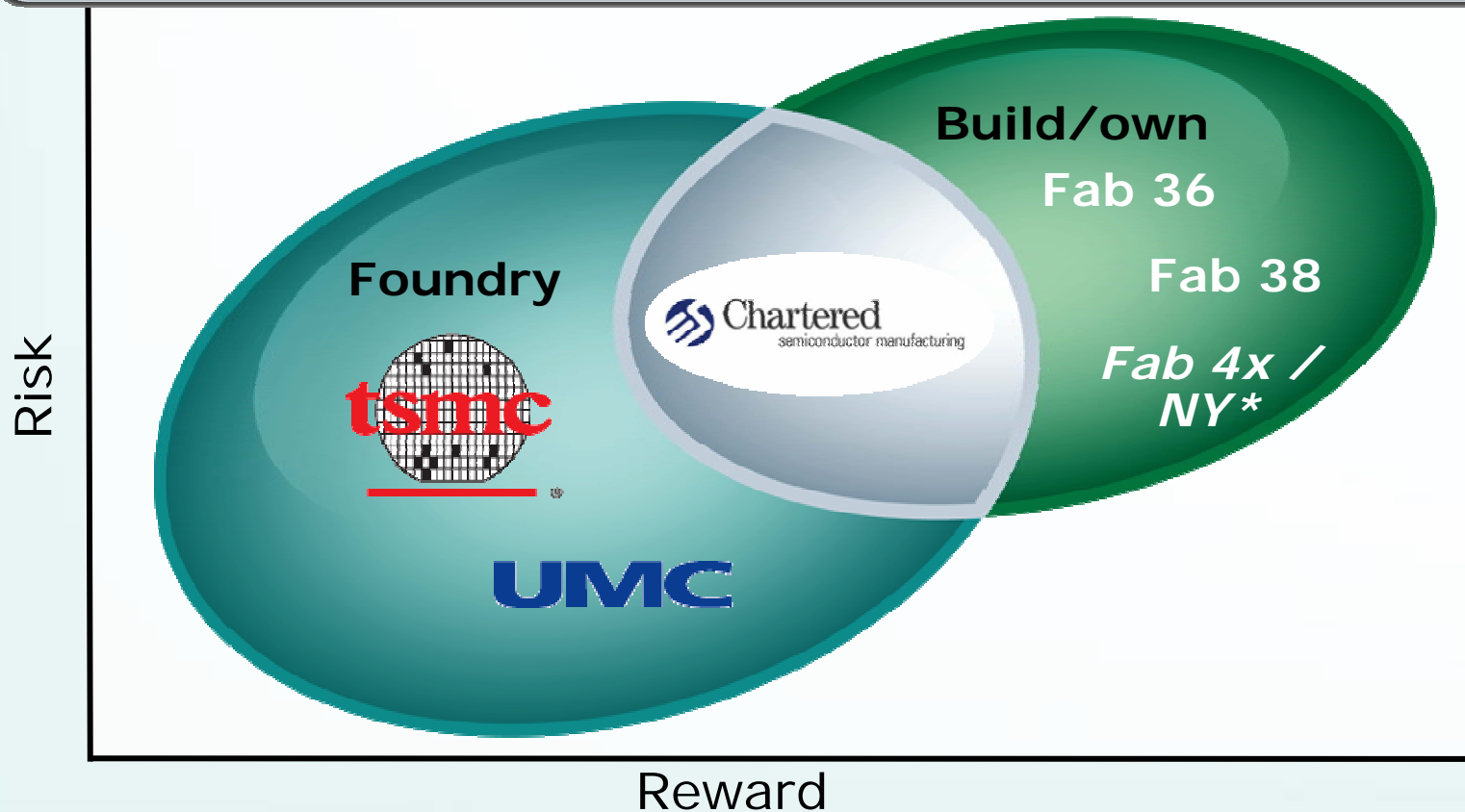
Shared return

- AMD wafers drive IBM learning curve
- Current generation: 45nm
 - High-performance, power-efficient SOI technology
- Next generations: 32nm and 22nm
 - Continued performance-per-watt leadership
 - Air-Gap, Ultra-low-k and “gate first” high-k / metal gate



Positioned for Success

- Asset Smart manufacturing today
- Balance in-house capabilities and foundry relationships



* Potential AMD Fab facility

Fab36

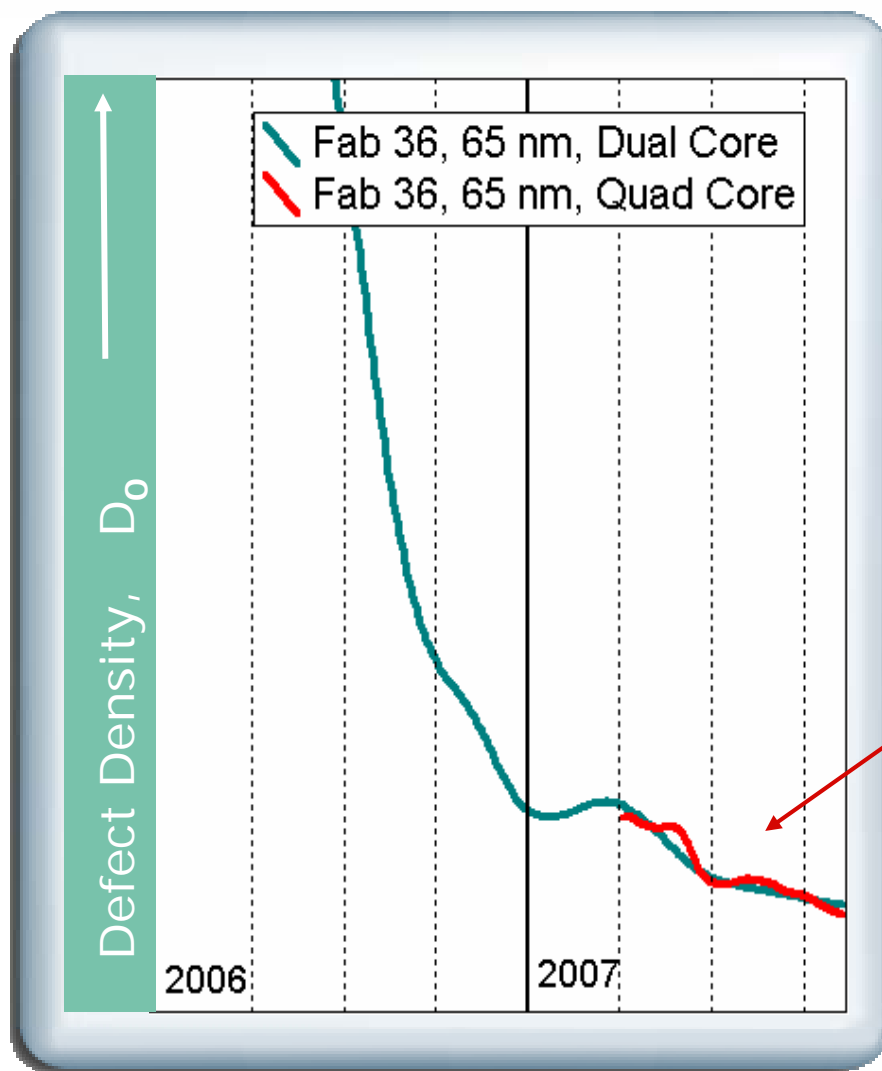
- 300mm ramp completed and on schedule
- Lean techniques driving efficiency
- Fully transitioned to 65nm, high manufacturing yields continue
- 45nm pilot lines running today
- Ramping 45nm in 1H08

Fab30/Fab38

- Last 200mm wafer out of Fab 30, November '07
- Initial 300mm tools in Fab 38 and complementing Fab 36 production
- Fab 38 transition to independent 300mm fab on track for '09
- New "Bump and Test" facility complete and fully operational



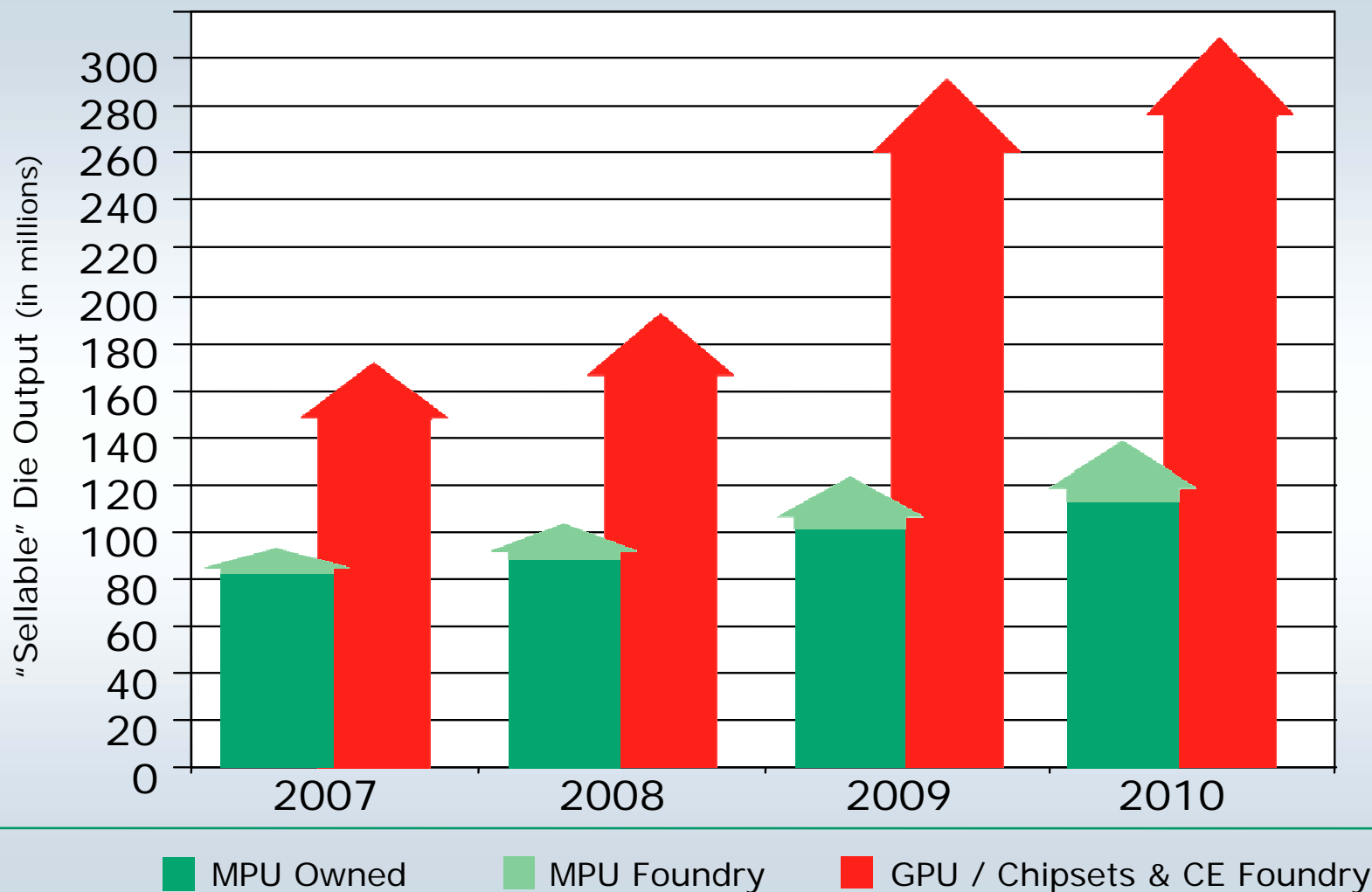
65nm Quad-Core Yields



Continuous yield improvement program drives 65nm defects down to lowest level in AMD's history

Quad-core production yield well in line with dual-core

Executing for Maximum Advantage



ATI Die Output is average 10x10 die size

Established Strategic Relationships with Top 3 Foundries



TSMC Fab 14, Tainan, Taiwan



UMC Fab 12A, Tainan



UMC Fab 12i, Singapore



TSMC Fab 12, Hsinchu, Taiwan



Chartered Fab 7

Full Production in 65nm with TSMC

Volume Production in 5 different 300mm facilities

Ramping 55nm in 4Q07

AMD & Chartered

"Flex Capacity" in Action

All milestones achieved ahead of schedule

65nm transition Complete

Powered by APM technology

Chartered Fab 7



Shared objective

- High-performance graphics/chipset/SoC production on leading edge bulk silicon technology

Shared investment

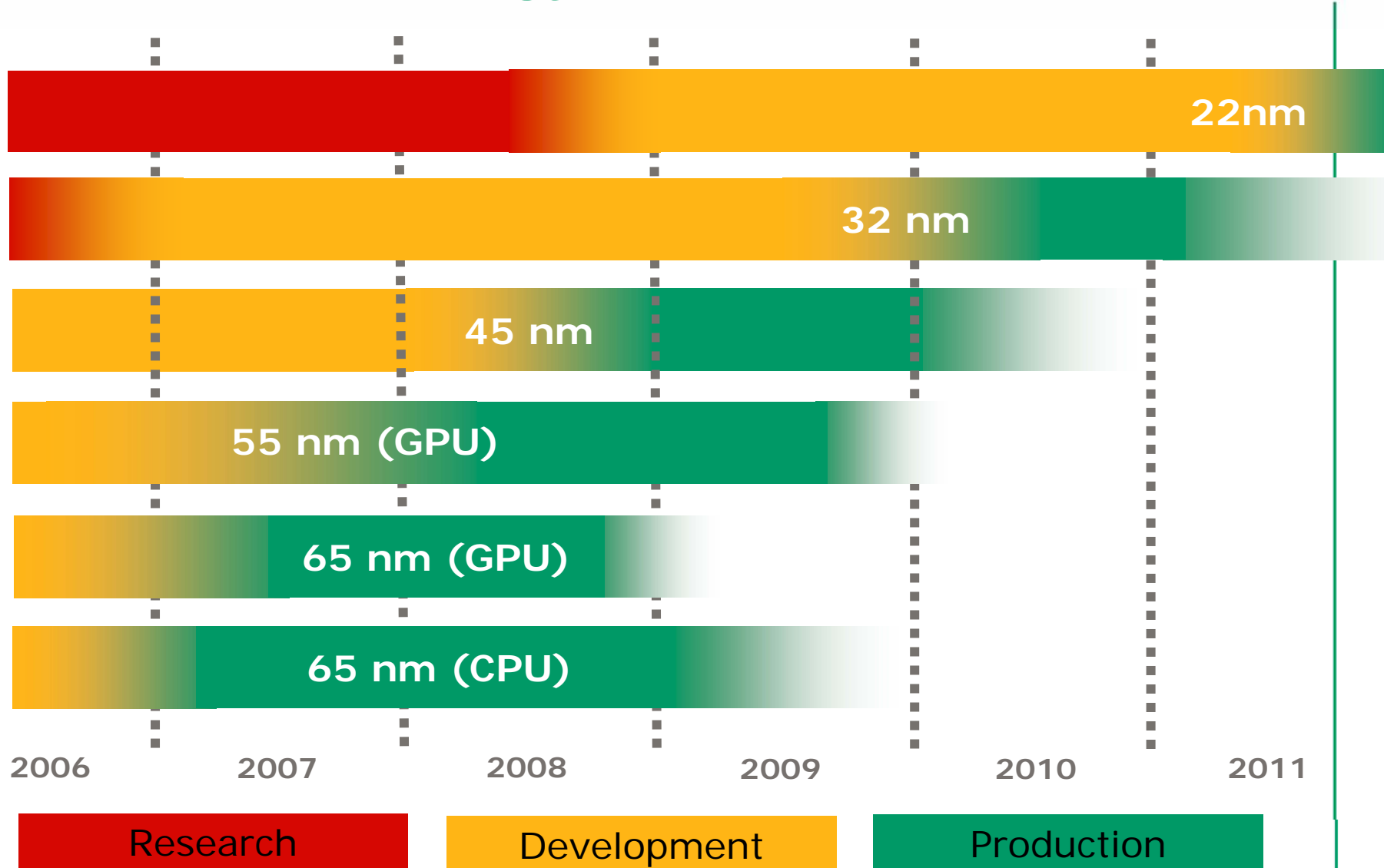
- Collaboration between design teams to maximize yield on leading-edge process nodes

Shared return

- 2 million wafers shipped (Q207)
- Maximum yields on premium products
- In partnership for almost 10 years
- Continued collaboration on leading-edge technology



Process Technology Roadmap



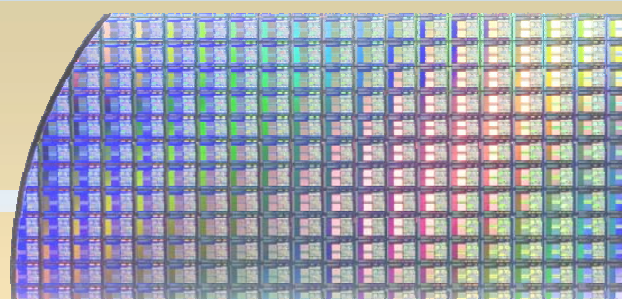
45nm Technology On-Track

Jointly Developed

- Jointly developed by IBM and AMD

Efficiency

- Ramped Immersion lithography
 - Reduces cost and complexity
- Strained silicon and ultra-low-K dielectrics
 - Ability to further enhance with High-k/metal gate devices at 45nm



Schedule – On Track

- Accelerated 45nm investment in 2H07
- Starting 45nm ramp in Fab 36 in 1H08
- Shipping 45nm product in 2H08

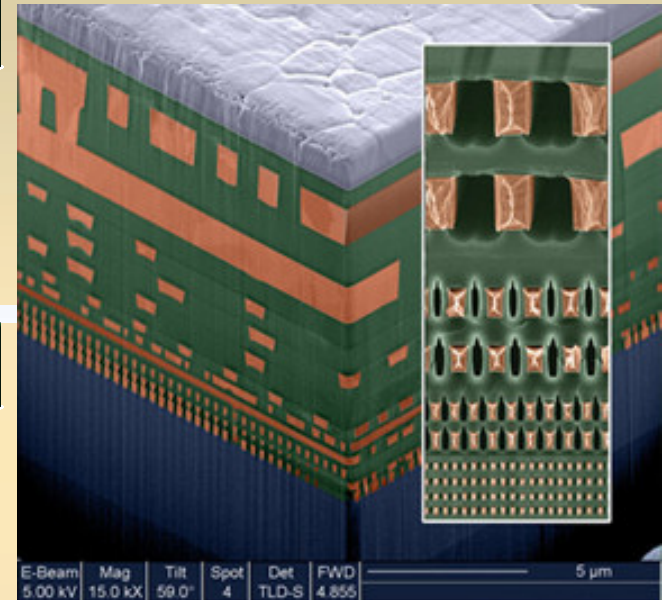
32nm Technology

Joint Development

- A product of the expanded research partnership with IBM
- Efficient, “Gate First” High-k / Metal Gate, Yielding 32nm SRAMs now

Performance and Power Efficiency

- High-k/Metal Gate transistor technology
- Combined Ultra-low-k and Vacuum Air-Gap technology
 - Greater than 30% reduction in interconnect capacitance
 - Anticipated 10% improvement in chip speed and 10% decrease in energy consumption
- Extending leadership in immersion lithography



Summary

1 Execution of AMD R&D technology model on-schedule

2 Manufacturing efficiency high and productivities ahead of plan allowing CAPEX reductions

3 Flexible capacity in place at Chartered (MPUs) and TSMC (GPUs & CE)

4 Asset Smart strategy in-place and expanding

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